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A 16K Electronically Erasable Nonvolatile Memory

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SESSION XII: ROMs, PROMs AND EROMs

THPM 12.6: A 16Kb Electrically Erasable Nonvolatile Memory

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FLOATING GATE STRUCTURES have been highly successful as nonvolatile devices because of their compatibility with silicon gate processing and their excellent charge retentivity with applied voltage at operating temperature. The accepted method of erasure in the commercial marketplace is ultra-violet light (EPROM)[1], although proposals have been made to erase electrically by avalanche injection of holes[2], electron tunneling[3,4], or a combination of both[5]. These methods, however, have typically suffered from poor reproducibility and very fast wearout during program/erase cycling.

To realize nonvolatile devices which can be erased electrically with high program/erase endurance, many have resorted to MNOS structures[6] which are programmed and erased by direct tunneling through a thin oxide. In this approach, charge is stored in traps within the nitride dielectric. A major problem with this approach is that the properties of the nitride/oxide dielectric are difficult to control and are adversely affected by normal silicon gate processing. Furthermore, the threshold voltages of these structures are vulnerable to disturbance by even small applied voltages and data retention is not easily guaranteed for long periods (years).

The device reported (FLOTOX, for *f*loating gate *t*unnel *o*xide) retains the processing and the retention advantages of floating gate over MNOS while solving the traditional endurance problem. This is accomplished by utilizing an oxide less than 200Å thick between a floating poly gate and an N^+ region, as shown in Figure 1. In FLOTOX both program and erase are accomplished by tunneling[7] of electrons through the tunnel oxide using voltages of less than 25V. A typical endurance plot for a single cell appears in Figure 2. This shows that the threshold window remains open beyond 100,000 cycles. Also by keeping voltages low during read, this structure can retain charge over 10 years under full power, at operating temperatures. There is no refresh requirement no matter how many read accesses are made.

The FLOTOX cell configuration, shown in Figure 3, uses two devices, a select transistor and a memory transistor. Cell area is $0.85mil^2$. Clearing of the memory is accomplished by programming every device in a row. This is done by selecting a row and raising the program line to VPP, which attracts electrons to the floating gate. Writing is accomplished by erasing selected bits within a word. This is done by again selecting a row, but now the program line is held at zero volts while selected columns go to VPP. Electrons are thus removed from the floating gates of the selected devices.

Figure 4 shows the 16K chip, which is arranged as 2K/8b words. It is packaged with 24 leads with a pinout identical to the 16K EPROM*. The chip is automatically powered down until selected ($\overline{CE}$ low). Read is accomplished by selecting the part and enabling the output buffers ($\overline{OE}$ low). On the other hand, selecting the part and taking VPP to 20V for 10ms puts the chip in write mode and writes a word. If the incoming data are all 1's, then the chip automatically goes into clear mode and clears the addressed word. Thus, a clear-write sequence requires merely two 10ms writes, first all 1s, then the data desired. If clearing of the entire chip is desired, this can be accomplished with one 10ms pulse by applying VPP to $\overline{OE}$ as well as the VPP pin with the chip selected. This approach allows a wide variety of functions while maintaining simple control and complete EPROM compatibility.

FLOTOX utilizes a new high performance N-channel two-level-poly silicon gate technology with channel lengths of 3.5μ. Access times for the 16K FLOTOX E^2PROM are below 200ns as shown in Figure 5. This allows use of the device with the newer microprocessors which operate in the 5-8MHz range without wait states. Other features of the 16K E^2PROM are listed in the table.

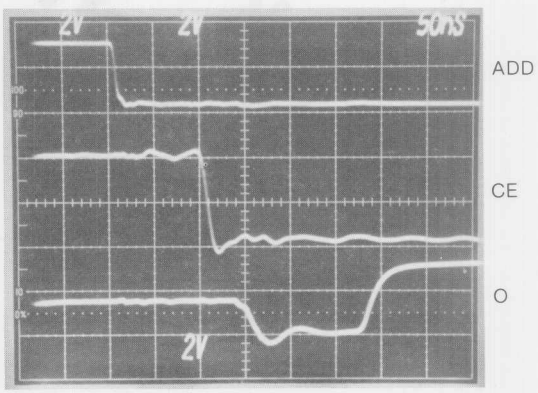


FIGURE 5—Access time for E^2PROM.

[†]Current Address: Hughes Research, Malibu, CA

*2716.

[1]Salsbury, P.J., Morgan, W.L., Perlegos, G. and Simko, R.T., "High Performance MOS EPROMs Using A Stacked Gate Cell", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 186; Feb., 1977.

[2]Gosney, W.M., "DIFMOS — A Floating-Gate Electrically Erasable Nonvolatile Semiconductor Memory Technology", *IEEE Transactions on Electron Devices*, ED-24, p. 594; May, 1977.

[3]Gulterman, D.C., Rimari, I.H., Halvorson, R.D., McElroy, D.J. and Chan, W.W., "Electrically Alterable Hot-Electron Injection Floating Gate MOS Memory Cell With Series Enhancement", *IEDM Technical Digest*, p. 340; Dec., 1978.

[4]Harari, E., Schmitz, L., Troutman, B. and Wang, S., "A 256-Bit Nonvolatile Static RAM", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 108; Feb., 1978.

[5]Scheibe, A. and Schulte, H., "Technology of a New N-Channel One-Transistor EAROM Cell Called SIMOS", *IEEE Transactions on Electron Devices*, ED-24, p. 600; May, 1977.

[6]Hagiwara, T., Kondo, R., Yatusuda, Y., Minami, S. and Itoh, Y., "A 16Kb Electrically Erasable Programmable ROM", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 50; Feb., 1979.

[7]Lenzlinger, M. and Snow, E.H., "Fowler-Nordheim Tunnelling into Thermally Grown SiO_2", *J. of Applied Physics*, 40, p. 278-283; Jan., 1969.

	16K E^2PROM	*16K EPROM*
Configuration	2K X 8	2K X 8
Package	24 pin	24 pin
Power Supplies		
read mode	+5	+5
clear/write	+5, +20	+5, +25
Write		
method	tunnel injection	hot electron injection
time/word	10ms	50ms
Clear		
method	tunnel ejection	UV light
time/word	10ms	–
time/chip	10ms	30 min
Access Time	200ns	450ns
Power Dissipation		
active	500mW	550mW
standby	100mW	100mW
Data Retention	10 years	10 years
Refresh Requirement	None	None

TABLE 1

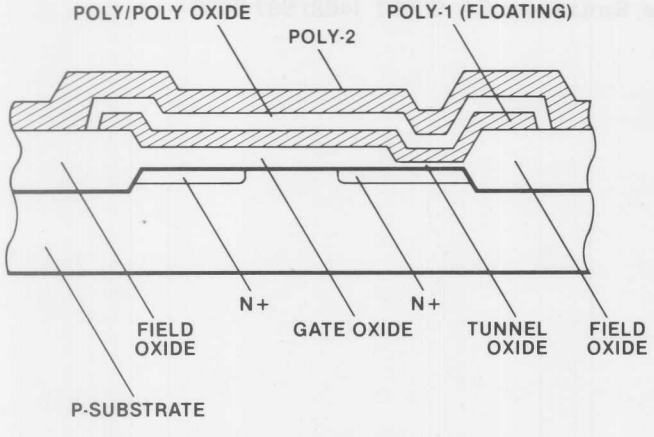


FIGURE 1—Cross section of memory transistor.

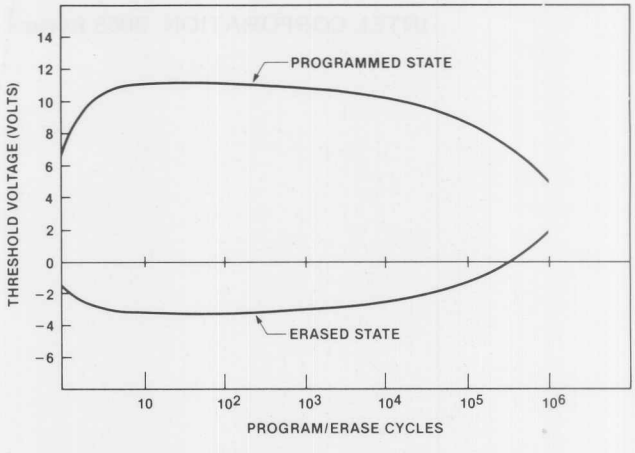


FIGURE 2—Program/erase endurance for single cell.

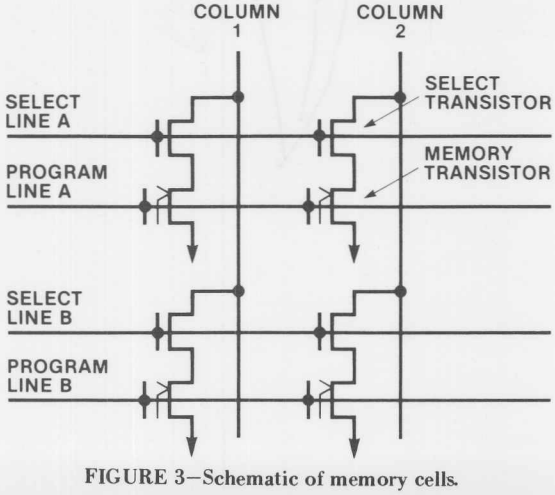
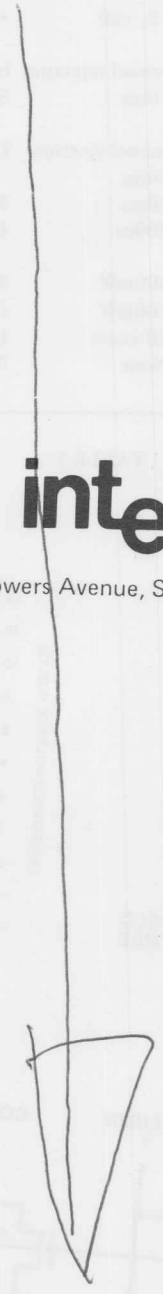


FIGURE 3—Schematic of memory cells.



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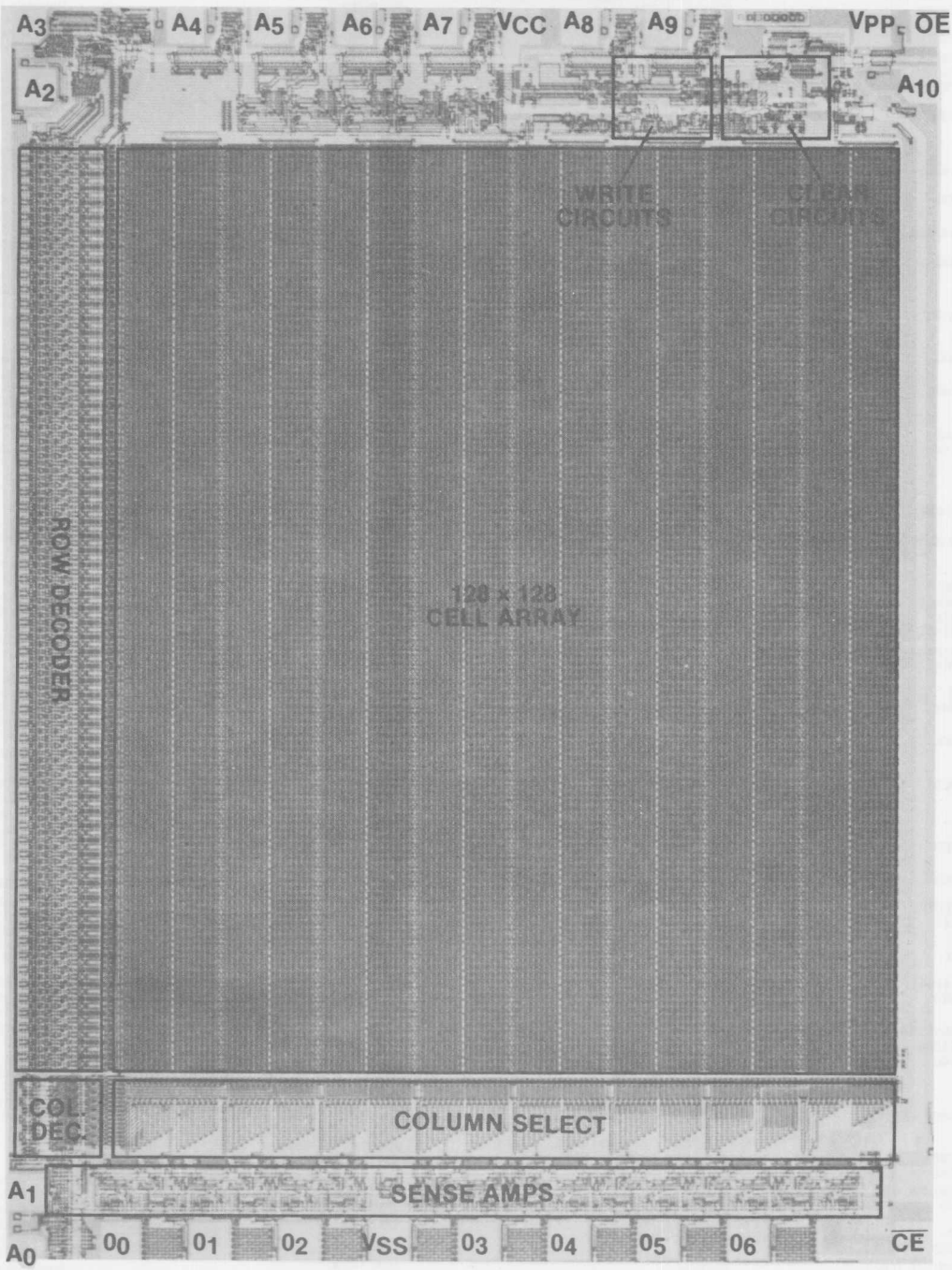

FIGURE 4—Photograph of 16Kb E^2PROM.

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